

## AMENDMENTS TO THE CLAIMS

1        1. (Original) An integrated circuit, comprising:  
2              a sensor operable to detect performance variations of an individual circuit in said  
3              integrated circuit, said performance variation being related to aging of said  
4              integrated circuit; and

5              a compensation circuit operable to change the operating characteristics of said  
6              individual circuit to compensate for said performance variation in  
7              accordance with an aging-versus time performance curve.

1        2. (Original) The integrated circuit of claim 1, wherein the individual  
2              circuit comprises a phase-locked loop.

1        3. (Currently Amended) ~~The integrated circuit of claim 2, An integrated circuit,~~  
2              comprising:

3              a sensor operable to detect performance variations of an individual circuit in said  
4              integrated circuit, wherein the individual circuit comprises a phase-locked  
5              loop, and wherein said performance variation is related to aging of said  
6              integrated circuit; and

7              a compensation circuit operable to change the operating characteristics of said  
8              individual circuit to compensate for said performance variation in  
9              accordance with an aging-versus time performance curve, wherein the  
10             compensation circuit comprises a charge pump having multiple legs that can  
11             be selectively enabled to change the performance characteristics of said  
12             phase-locked loop.

1        4. (Currently Amended) The integrated circuit of claim 2 3, wherein said  
2              compensation circuit comprises a power supply controlled by digital control words to  
3              selectively change the operating characteristics of said phase-locked loop.

1           5. (Currently Amended) The integrated circuit of claim 2 3, comprising a ring  
2 oscillator operable to approximate the effects of NBTI and to generate a compensation  
3 signal corresponding thereto.

1           6. (Original) The integrated circuit of claim 5, wherein said compensation  
2 signal is used to generate digital control words to control operation of a power supply.

1           7. (Original) The integrated circuit of claim 6, wherein said power supply  
2 is operable to control operation of a voltage controlled oscillator in said phase-locked loop.

1           8. (Currently Amended) The integrated circuit of claim 4 3, wherein said  
2 individual circuit is a delay-locked loop.

1           9. (Original) The integrated circuit of claim 8, wherein the compensation  
2 circuit comprises:

3           a dummy delay line operable to generate a dummy delay line clock signal;  
4           a reference source operable to generate a reference clock signal; and  
5           a comparator operable to compare the dummy delay line clock signal and the  
6           reference clock signal and to generate a control signal therefrom.

1           10. (Original) The integrated circuit of claim 9, further comprising a power  
2 supply controller operable to control operation of the delay line of said delay-locked loop in  
3 response to said control signal.

1           11. (Original) The integrated circuit of claim 10, wherein said power supply  
2 controller controls operation of said delay line by generating a digital power supply control  
3 word (VDD\_DLL).

1           12. (Original) A method for controlling operation of an integrated circuit,  
2 comprising:

3           detecting performance variations of an individual circuit in said integrated circuit,  
4           said performance variation being related to aging of said integrated circuit;  
5           and  
6           generating a compensation signal to change the operating characteristics of said  
7           individual circuit to compensate for said performance variation in  
8           accordance with an aging-versus time performance curve.

1           13. (Original) The method of claim 12, wherein the individual circuit  
2 comprises a phase-locked loop.

1           14. (Currently Amended) The method of claim 13, A method for controlling  
2 operation of an integrated circuit comprising:

3           detecting performance variations of an individual circuit in said integrated circuit,  
4           wherein the individual circuit comprises a phase-locked loop and wherein  
5           said performance variation is related to aging of said integrated circuit; and  
6           generating a compensation signal to change the operating characteristics of said  
7           individual circuit to compensate for said performance variation in  
8           accordance with an aging-versus time performance curve, wherein said  
9           compensation signal is generated by a charge pump having multiple legs that  
10          can be selectively enabled to change the performance characteristics of said  
11          phase-locked loop.

1           15. (Currently Amended) The method of claim 13 14, wherein compensation  
2           signal is generated by a power supply controlled by digital control words to selectively  
3           change the operating characteristics of said phase-locked loop.

1           16. (Currently Amended) The method of claim 13 14, wherein said  
2           compensation signal is generated by a ring oscillator operable to approximate the effects of  
3           NBTI and to generate a compensation signal corresponding thereto.

1           17. (Original) The method of claim 16, wherein said compensation signal is  
2 used to generate digital control words to control operation of a power supply.

1           18. (Original) The method of claim 17, wherein said power supply is  
2 operable to control operation of a voltage controlled oscillator in said phase-locked loop.

1           19. (Currently Amended ) The method of claim ~~12~~ 14, wherein said individual  
2 circuit is a delay-locked loop.

1           20. (Original) The method of claim 19, wherein the compensation circuit  
2 comprises:

3           a dummy delay line operable to generate a dummy delay line clock signal;  
4           a reference source operable to generate a reference clock signal; and  
5           a comparator operable to compare the dummy delay line clock signal and the  
6           reference clock signal and to generate a control signal therefrom.